This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Cancelled)

2. (Currently amended) A[[The]] semiconductor device ~~as in claim 1~~ having low metallization series resistance, the semiconductor device comprising:

a metallization structure formed on a semiconductor substrate;

an under bump metallurgy (UBM) layer formed over said metallization structure; and

a conductive bump formed directly over said UBM layer and directly over the metallization structure,

wherein a largest linear dimension of said UBM layer is greater than a diameter of said conductive bump, said metallization structure comprises a top metallization layer, said UBM layer is formed over the top metallization layer, and a thickness of said top metallization layer is substantially smaller than a thickness of said UBM layer.

3. (Previously presented) The semiconductor substrate as in claim 2 wherein said top metallization layer comprises aluminum.

4. (Currently amended) The semiconductor device as in claim [[1]]2 wherein said UBM layer comprises (i) a bottom layer comprising a metal, said bottom layer adhering to said metallization structure, (ii) a middle layer comprising a barrier metal, and (iii) a top layer comprising a conductive solderable metal.

5. (Previously presented) The semiconductor device as in claim 4 wherein said bottom layer metal comprises at least one of aluminum, titanium, and chromium.

6. (Previously presented) The semiconductor device as in claim 4 wherein said barrier metal comprises nickel.

7. (Previously presented) The semiconductor device as in claim 4 wherein said barrier metal comprises vanadium.

8. (Previously presented) The semiconductor device as in claim 4 wherein said solderable conductive material comprises copper.

9. (Previously presented) The semiconductor device as in claim 4 wherein said solderable conductive material comprises gold.

10. (Previously presented) A semiconductor device having low metallization series resistance, the semiconductor device comprising:

a top metallization layer formed on a semiconductor substrate;

a UBM layer formed over said top metallization layer; the UBM layer comprising (i) a bottom layer comprising at least one of aluminum and chromium, said bottom layer adhering to said metallization structure, (ii) a middle layer comprising vanadium, and (iii) a top layer comprising a conductive solderable metal; and

a conductive bump formed over said UBM layer

wherein a thickness of said top metallization layer is substantially smaller than a thickness of said UBM layer, and a largest linear dimension of said UBM layer is greater than a diameter of said conductive bump.

11. (Currently amended) A[[The]] semiconductor device ~~as in claim 10~~ having low metallization series resistance, the semiconductor device comprising:

a top metallization layer formed on a semiconductor substrate;

a UBM layer formed over said top metallization layer; the UBM layer comprising (i) a bottom layer comprising at least one of aluminum and chromium, said bottom layer adhering to said metallization structure, (ii) a middle layer comprising vanadium, and (iii) a top layer comprising a conductive solderable metal; and

a conductive bump formed over said UBM layer,

wherein a thickness of said top metallization layer is substantially smaller than a thickness of said UBM layer, and a largest linear dimension of said UBM layer is greater than a diameter of said conductive bump and said top metallization layer comprises aluminum.

12.–14. (Cancelled)

15. (Previously presented) The semiconductor device as in claim 11 wherein said barrier metal comprises nickel.

16. (Cancelled)

17. (Previously presented) The semiconductor device as in claim 11 wherein said conductive solderable metal comprises copper.

18. (Previously presented) The semiconductor device as in claim 11 wherein said conductive solderable metal comprises gold.

19. (Previously presented) The semiconductor device as in claim 1 wherein the UBM layer consists essentially of a single layer.